

# A 400 MHz DDS Core Unit

## General

The Direct Digital Synthesis (DDS) Unit described in this document is based on the [Analog Devices](#) AD9951/54 family chips featuring advanced technology, high speed 14 bit Digital to Analog Converter, capable of generating a frequency-agile analog output sinusoidal waveform at up to 200 MHz with a fine tuning resolution of 32 bits.

The Unit consists of a 2-layer pcb providing maximum flexibility in a minimum size, it includes room and facilities for: the 3,3 Volt Digital Vdd regulator, the 1,8 Volt Analog Vdd regulator, Quartz or On Board / External Oscillator, Low-Pass Filtering and a Wide-Band linear Amplifier. The Unit can be interfaced to a micro based controller through a suitable 6 pin connector. The DDS Unit Circuit Diagram is drawn on Fig. 1, while Fig. 2 shows the actual Printed Circuit Board Top Layer. This Project has been developed thanks to the strictly collaborated work of [iCCG](#), Giuliano and [iGLLU](#), Giancarlo.

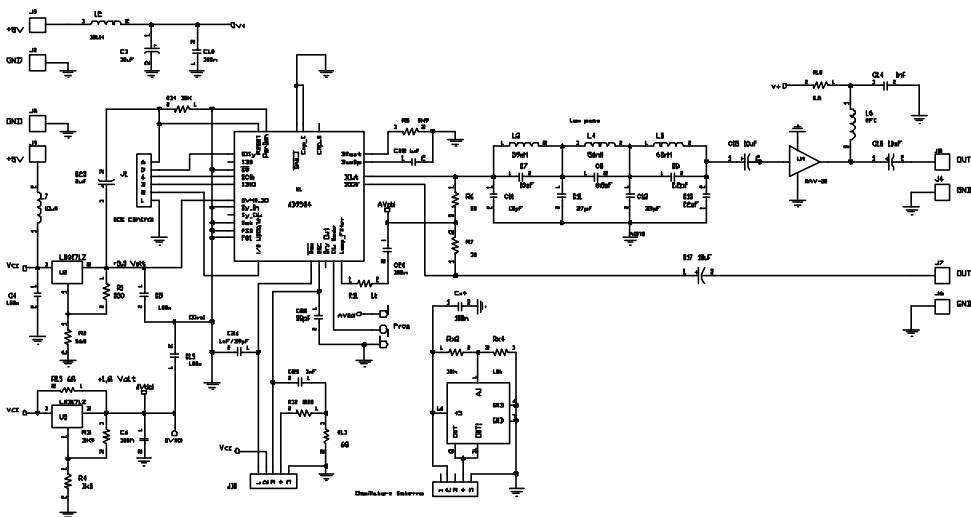


Fig. 1 DDS Unit Circuit Diagram

## Circuit Diagram Analysis

The core of the circuit is the 48 pin chip, it can be an AD9951 or an AD9954.

The connector J1 interfaces the DDS Unit to the microcontroller subsystem; it provides connection to the Ground, I/O Update, SDIO, SClck, I/O Sync and Reset signals. As an alternative, the Reset can be done by using the R14-C23 network. The I/O Sync signal, if unused, can be tied to the Reset signal.

J8 and J9 interface the power source Vcc at 5 Volt which feeds the 3,3 Volt and the 1,8 Volt LM317LZ regulators. As an alternative, the board can be powered at 3,3 Volt (replace U2 with a short of pin 2-3) or 1,8 Volt only (short U2 and U3).

The system oscillator can be serviced by a single (20-30 MHz) Quartz or an External clock source. The Quartz must be connected to the connector J10 pins 1 - 3 and related 39 pF capacitors C24 and C26. The Prog pad must be connected to the "Q" side.

When the External clock source is selected the Prog pad must be connected to the "E" side and two alternatives are possible: to use the on board SMT Oscillator or to connect an auxiliary board to J10. In both cases C24 must be increased to 1 nF, the Vcc power is made available at the connector J10 pin 2 and the Oscillator Output is routed to the connector J10 pin 4.

Note that the Oscillator Output signal needs to be reduced within a 0 dbm limit and DC decoupled.

Both the DAC outputs have been made available, one as OUTb (through R7 and C17) and the second as OUTa, this last can be routed to a 3-cell Low-Pass elliptic filter (C10, L3, C7, C11, L4, C8, C12, L5, C9, C13) and to the Linear Amplifier (U4).

## The Printed Circuit Board

The Fig.2 picture shows the DDS Unit Printed Circuit Board Top Layer and the related Silkscreen labels. The actual dimensions of the pcb are 27 x 67 mm.

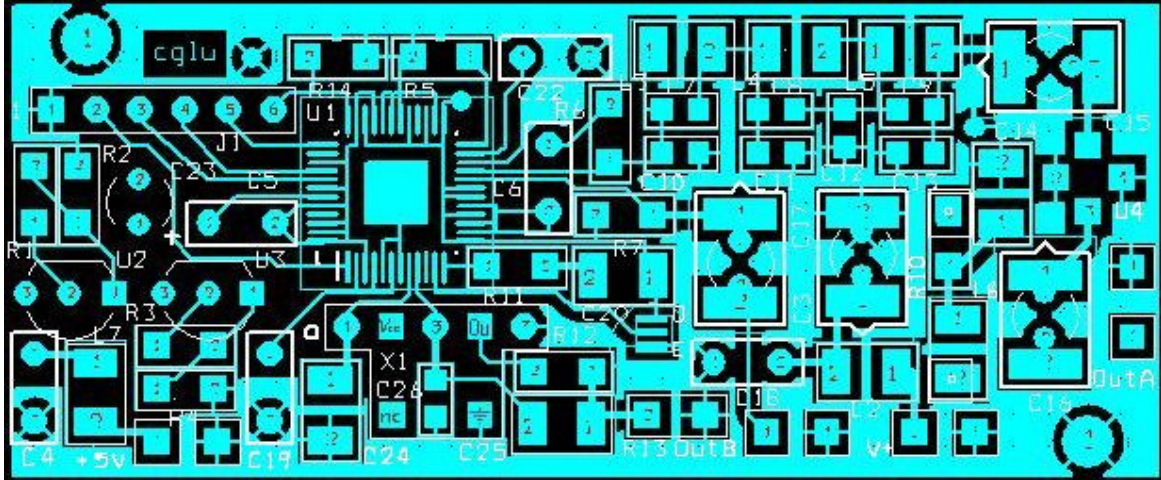


Fig. 2 DDS Unit Printed Circuit Board Top Layer

On the left top of the pcb is located the J1 connector, it provides the necessary interface signals to the microcontroller subsystem. As an option, the I/O Sync signal (pin 5) can be tied to the Reset signal; the Reset signal can be generated either locally, by placing on the capacitor C23 and the resistor R14 or by the microcontroller subsystem, but in this case C23 must be removed.

U2 provides the regulation for the 3,3 Volt Digital Vdd power, while U3 for the 1,8 Volt Analog Vdd power, both of them are fed by the Vcc (normally + 5 Volt) power net Vcc is also routed to the connector J10 pin 2 in order to power the External Oscillator.

When a single Quartz is used it shall be connected to X1 pins (J10, 1 and 3), the capacitors C24 and C26 (39 pF) must be placed on and the Prog pad shall be tied to the "Q" side (AVdd); R12 and R13 are unnecessary, C25 must be excluded.

When the External Oscillator is selected C24 shall be increased to 1nF while C26 must be excluded, the Prog pad shall be tied to the "E" side (GND), C25 (DC decoupling) shall be placed on and the attenuator (R12, R13) shall be used in order to forward a proper power level (0 dbm) to the REF CLOCK input. Practically any kind of external clock source can be interfaced at the J10 connector. As for an additional option an SMT on board oscillator ([CFPS-72](#)) can be used, it shall use the Vcc, Ou, and GND pads.

On the right top of the pcb a three cell filter structure has been provided, it can house the suggested LowPass elliptic filter featuring an excellent response from DC up to 200 MHz, derived from the [Analog Devices](#) application Document AD9954\_RevC\_schem.pdf. However different kind of custom filtering circuits can be housed within the same room.

The right end of the pcb houses the Linear Amplifier (U4) and the related OutA circuitry.

A [Mini-Circuits](#) MAV-11 can be used as U4, the network L6, R10, C14 provides suitable biasing for common applications. In wide band applications the Linear Amplifier U4 must be polarized by a single resistor and a proper V+ voltage (12 Volt, 220 ). For this purpose R10 and L6 can be replaced by an axial (0,5 Watt) resistor which can fit into the two specific "passing" pads.

The C3, C15, C16 and C17 polarized capacitors show a double face footprint where either SMT or more common classic capacitors can be housed. The capacities of C15, C16 and C17 also affect the band-pass figures of the overall Unit: higher capacities provide larger band-pass on the lower end but sometime they show a not so good behaviour at the highest frequencies.

In the case a higher Vcc voltage is used (for instance the same as V+) the regulator U3 could become overheated, under these circumstances a shunt resistor R15 can be placed on the Bottom side of the pcb, thus reducing the current flow inside U3.